ABSTRACT OF THE DISCLOSURE

A system comprises a plurality of memory controllers connected to a memory bus. Each memory controller is able to generate memory requests on the memory bus according to a predetermined priority scheme. One priority scheme is a time slot priority scheme, and another priority scheme is a request-select priority scheme. The plurality of memory controllers are able to monitor memory requests generated by another memory controller in performing memory-related actions, such as memory requests (read or write), read-modify-write transaction, and cache coherency actions. In one arrangement, the memory bus is a Rambus channel.